IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): ~~A semiconductor integrated circuit device comprising:~~

~~a first interconnection which is made of materials containing copper as a principal ingredient and has a given width, length, thickness and volume;~~

~~a second interconnection which is made of materials containing copper as a principal ingredient and provided above said first interconnection; and~~

~~at least one via contact which is made of materials containing copper as a principal ingredient and through which said first interconnection and said second interconnection are electrically connected to each other, said at least one via contact including one via contact which is provided when one of the width and the volume of said first interconnection is not larger than a given value and a plurality of via contacts, which are arranged at regular intervals, each of which is not larger than a given value, in a predetermined region of said first interconnection,~~ A method of fabricating a semiconductor integrated circuit device, the semiconductor integrated circuit device including a first interconnection which is made of materials containing copper as a principal ingredient and has a given width, thickness and volume, at least one via contact which is made of materials containing copper as a principal ingredient, said at least one via contact being electrically connected to the first interconnection, and a second interconnection which is made of materials containing copper as a principal ingredient, the second interconnection being electrically connected to said at least one via contact,

the method comprising:

forming one via contact as said at least one via contact when one of the width and volume of the first interconnection is not larger than a given value, and forming a plurality of

via contacts in a predetermined region of the first interconnection as said at least one via contact, said plurality of via contacts being arranged at regular intervals, when one of the width and the volume of said first interconnection exceeds a given value.

Claim 2 (Currently Amended): The method of fabricating a semiconductor integrated circuit device according to claim 1, wherein voids are unevenly centralized in a contact ~~position~~ portion of said first interconnection to which said at least one via contact is ~~connected~~ formed.

Claim 3 (Currently Amended): The method of fabricating a semiconductor integrated circuit device according to claim 1, wherein said one via contact is provided when the width and the length of said first interconnection are each 2 μm or less, and said one via contact has a diameter of 0.2 μm or smaller.

Claim 4 (Currently Amended): The method of fabricating a semiconductor integrated circuit device according to claim 1, wherein said plurality of via contacts are provided when the width and the length of said first interconnection each exceed 2 μm, and each have a diameter of 0.2 μm or smaller.

Claim 5 (Currently Amended): The method of fabricating a semiconductor integrated circuit device according to claim 1, the semiconductor integrated circuit device further ~~comprising~~ including a third interconnection which is made of materials containing copper as a principal ingredient and being formed in contact with one end of said first interconnection in a direction of the length of said first interconnection such that the third interconnection is

flush with the first interconnection, the third interconnection having a given width, length, thickness and volume,

wherein said one via contact is provided when one of the width and the volume of said third interconnection is not larger than a given value.

Claim 6 (Currently Amended): The method of fabricating a semiconductor integrated circuit device according to claim 5, wherein the width and the length of said third interconnection are each 2 μm or less and said one via contact has a diameter ~~that is not larger~~ of less than 0.2 μm.

Claim 7 (Currently Amended): The method of fabricating a semiconductor integrated circuit device according to claim 1, the semiconductor integrated circuit device further ~~comprising~~ including a third interconnection which is made of materials containing copper as a principal ingredient and formed in contact with one end of said first interconnection in a direction of the length of said first interconnection such that the third interconnection is flush with the first interconnection, the third interconnection having a given width, length, thickness and volume,

wherein said plurality of via contacts are arranged at regular intervals, each of which is not smaller than a given value, in a predetermined region of said first interconnection when one of the width and the volume of said third interconnection exceeds a given value.

Claim 8 (Currently Amended): The method of fabricating a semiconductor integrated circuit device according to claim 7, wherein the width and the length of said third interconnection each exceed 2 μm and said plurality of via contacts each ~~have~~ has a diameter ~~that is~~ of not larger than 0.2 μm.

Claim 9 (Currently Amended): The method of fabricating a semiconductor integrated circuit device according to claim 1, wherein the predetermined region of said first interconnection is a void effective diffusion region in which voids included in said first interconnection are centralized by diffusion on a bottom of said via contact to cause a contact failure in said via contact.

Claim 10 (Currently Amended): The method of fabricating a semiconductor integrated circuit device according to claim 9, wherein said void effective diffusion region is defined by an almost circular region ~~at~~ having a radius ~~of~~ R ~~from~~ at a center of the bottom of ~~one of said plurality of via contacts in~~ the via contact at which the largest number of voids are centralized.

Claim 11 (Currently Amended): The method of fabricating a semiconductor integrated circuit device according to claim 10, wherein the radius R is given by $R = (F \cdot t)^{0.5}$ where F is a diffusion coefficient of the voids and t is diffusion time.

Claim 12 (Currently Amended): The method of fabricating a semiconductor integrated circuit device according to claim 10, wherein the radius R is 25 μm.